4/4 B.Tech -SEVENTH SEMESTER

EC7T4B **Digital System Design** **Credits: 3**

Lecture: 3 periods/week **Internal assessment: 30 marks**
Tutorial: 1period/week **Semester end examination: 70 marks**

Prerequisites: Switching Theory and Logic Design (EC3T6)

Course Objectives:

- To analyze and design combinational and sequential logic circuits.
- To understand developing Verilog HDL code to describe and synthesize combinational & sequential logic circuits.

Learning Outcomes:

Student will be able to

- Design latches, flip-flops, and differentiate between synchronous and asynchronous circuit operation.
- Perform analysis of synchronous sequential circuits.
- Develop Verilog HDL implementations on the structured design of synchronous sequential circuits.
- Design algorithmic state machines (ASMs) for digital system design.

UNIT-I

Digital Logic Design Using Verilog HDL: Introduction to CAD Tools, Introduction to Verilog, Structural Specification of Logic Circuits, Behavioral Specification of Logic Circuits, Synthesis of Logic Functions Using Multiplexers, Multiplexer Synthesis Using Shannon's Expansion, Decoders , Demultiplexers Binary Encoders Priority Encoders , Code Converters , Verilog for Combinational Circuits ,The Conditional Operator, The If-Else Statement ,The Case Statement , The For Loop .Edge-Triggered D Flip-Flops , D Flip-Flops with Clear and Preset ,T Flip-Flop ,JK Flip-Flop.

UNIT-II

Arithmetic Circuits: Half Adder, Full Adder, Ripple- Carry Adder, Carry Look – Ahead Adder, Serial Adder , multiplication, Arithmetic Comparison Circuits and Design of Arithmetic Circuits Using Verilog .

UNIT-III

Synchronous Sequential Circuits: State Table , State Assignment ,Choice of Flip-Flops and Derivation of Next-State and Output Expressions ,State-Assignment Problem ,One-Hot Encoding ,Mealy State Model, Verilog Code for Moore-Type FSMs, Verilog Code for Mealy FSMs, Specifying the State Assignment in Verilog Code .State Minimization ,Design of a

Counter Using the Sequential Circuit Approach State Diagram and State Table for a Modulo-8 Counter ,State Assignment , Implementation Using D-Type Flip-Flops Implementation Using JK-Type Flip-Flops ,Algorithmic State Machine (ASM) Charts.

UNIT-IV

Asynchronous Sequential Circuits: Asynchronous Behavior, Analysis of Asynchronous Circuits, Synthesis of Asynchronous Circuits, State Reduction.

UNIT-V

SRAM and Timing Parameters: Static Hazards , Dynamic Hazards , Significance of Hazards, Flip-Flops and Registers with Enable Inputs ,Shift Registers with Enable Inputs, Static Random Access Memory(SRAM) ,SRAM Blocks in PLDs, Clock Skew ,Flip-Flop Timing Parameters, Asynchronous Inputs to Flip-Flops.

Learning Resources

Text Books:

1. Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog design", Tata McGraw Hill,2002

References:

1. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition,2003.
2. J. Bhaskar, "A Verilog Primer'', BSP, 2nd edition 2003.